33. (new) A semiconductor device comprising:

a semiconductor substrate including first and second memory cell areas;

the first memory cell area including a first field effect transistor comprising a first tunnel insulating film in contact with the substrate, a first floating gate in contact with the tunnel insulating film, a first dielectric layer in contact with the floating gate, a first control gate in contact with the dielectric layer, and first source/drain regions extending into the substrate;

the second memory cell area including a second field effect transistor comprising a second tunnel insulating film in contact with the substrate, a second floating gate in contact with the second tunnel insulating film, a second dielectric layer in contact with the second floating gate, a second control gate in contact with the second dielectric layer, and second source/drain regions extending into the substrate;

a connecting area capable of electrically connecting one of the first source/drain regions with one of the second source/drain regions, wherein the connecting area has an electric resistance which is lower than that of the first source/drain regions and lower than that of the second source/drain regions, and wherein the impurity concentration of the connecting area is higher than the impurity concentrations of the first source/drain regions and higher than the impurity concentrations of the second source/drain regions; and

a groove formed on the connecting area of the substrate, wherein no portion of the floating gate is positioned within the groove.--

REMARKS

Applicant has canceled claims 1-12 and 20-25 without prejudice, amended claim 13 without prejudice, and added new claims 30-33. Claims 13-19 and 26-33 are currently pending. Reexamination and reconsideration are respectfully requested. Claim 13 has been amended without prejudice to further prosecute the claim as originally filed at a later time.

Applicant notes that the Examiner did not appear to address Applicant's statement in response to the restriction requirement that MPEP section 803 states that "if the search and examination of an entire application can be made without serious burden, the examiner must examine it on the merits, even though it includes claims to independent or distinct inventions."

Applicant respectfully submits that the Examiner has not established that it would be an undue burden for the Examiner to examine claims 13-19 and 26-29 in the present application.

Claims 13-14 and 16 were rejected under 35 U.S.C. 102(e) or 103(a) as unpatentable over Hirayama (US 6,015,725). The rejection is respectfully traversed.

Applicant respectfully submits that the Examiner has cited no portion of the art the describes or suggests "sources and drains formed on the first and second cell areas at positions in contact with a common plane defined by a surface of the semiconductor substrate" as recited in claim 13, as amended. It appears that the sources and drains in the vertical transistor of Hirayama are not formed at positions such as recited in claim 13. Accordingly, applicant respectfully submits that the rejection of claim 13 and its dependent claims 14 and 16 be withdrawn.

New claims 30-33 have been added. Support for the new claims may be found throughout the specification and drawings and in the original claims. It is believed that no new matter has been entered.

Attached hereto is a marked-up version of the claim amendments made by the present amendment. The attached page is captioned "Version with markings to show changes made."

Reexamination and reconsideration are respectfully requested. If, for any reason, the application is not in condition for allowance, the Examiner requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

Alan S. Raynes

Dated: March 25, 2002

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on March 25, 2002.

Alan S. Raynes — **March 25, 2002**

Alan S. Raynes — **(Date)**

Version With Markings to Show Changes Made

Claim 13 was amended as follows:

13. (amended) A semiconductor device comprising:

tunnel insulating films, floating gates, dielectric films and control gates, all of which are laminated on first and second cell areas on a semiconductor substrate;

sources and drains formed on the first and second cell areas at positions in contact with a common plane defined by a surface of the semiconductor substrate;

a connecting area capable of electrically connecting one of the source and drain of the first cell area with one of the source and drain of the second cell area, wherein the connecting area has an electric resistance which is lower than any one of the sources and drains of the first and second cell areas.